

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

1. (Currently Amended) A microelectronic die substrate having an active side and a back side, comprising:

an active side interconnect disposed on the active side of the microelectronic die substrate;

a backside interconnect disposed on the backside of the microelectronic die, coupled to and in substantial vertical alignment with the active side interconnect; and

a redistributed interconnect of the backside interconnect disposed on the backside, coupled to and offset from the backside interconnect.

2. (Original) The substrate of claim 1, further comprising:

a metal layer having a first side and a second side;

a first dielectric layer adjacent to the first side of the metal layer;

a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;

a second dielectric layer adjacent to the second side of the metal layer; and

a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

3. (Original) The substrate of Claim 1, wherein the redistributed interconnect comprises:

a conductive trace coupled to and extending from the backside interconnect to a selected location;

a third dielectric layer overlaying the conductive trace; and

an aperture in the third dielectric layer substantially at or near the selected location.

4. (Original) The substrate of Claim 3, wherein the selected location for the redistributed interconnect corresponds to an interconnect on a second substrate.
5. (Original) The substrate of Claim 1, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.
6. (Currently Amended) A semiconductor device, comprising:
a carrier substrate having a bond pad;
a first microelectronic die substrate, the first microelectronic die substrate ~~comprising~~including,
an active side and a back side;
an active side interconnect, the active side interconnect disposed on the active side, coupled to the bond pad of the carrier substrate;
a backside interconnect disposed on the back side, coupled to and in substantial vertical alignment with the active side interconnect;
a redistributed interconnect of the backside interconnect, disposed on the backside, coupled to and offset from the backside interconnect; and
a second microelectronic die substrate electrically coupled to the redistributed interconnect of the first microelectronic die substrate.
7. (Original) The semiconductor device of claim 6, wherein the first substrate comprises:
a metal layer having a first side and a second side;
a first dielectric layer adjacent to the first side of the metal layer;
a first aperture in the first dielectric layer, the first aperture exposing a portion of the first side of the metal layer to define the active side interconnect;
a second dielectric layer adjacent to the second side of the metal layer; and
a via extending from the backside interconnect through the second dielectric layer to the second side of the metal layer to electrically couple the backside interconnect to the metal layer.

8. (Original) The semiconductor device of Claim 6, wherein the redistributed interconnect comprises:

a conductive trace coupled to and extending from the backside interconnect to a selected location;

a third dielectric layer overlaying the conductive trace; and

an aperture in the third dielectric layer at the selected location.

9. (Original) The semiconductor device of Claim 8, wherein the selected location for the redistributed interconnect corresponds to an interconnect on the second substrate.

10. (Cancelled)

11. (Currently Amended) The semiconductor device of claim 6, wherein the second substrate is coupled to the redistributed interconnect by a process selected from the group ~~including~~ consisting of reflow bonding, thermal compression bonding, ~~or and~~ ultrasonic bonding.

12. (Original) The semiconductor device of Claim 6, wherein the redistributed interconnect is not in vertical alignment with the backside interconnect.

13 – 25 (Withdrawn).